In the Claims:

Claims 1-10 are cancelled.

Please cancel Claims 11-21.

Claims 22-37 are cancelled.

Please cancel Claims 38-53.

54. (New) A method of manufacturing a semiconductor device, comprising:

forming an SiC layer in a reaction chamber;

forming a SiOC etch stop layer on the SiC layer in the reaction chamber with an SiOC formation process comprising:

flowing trimetholsilane (3MS) into and through the reaction chamber,

flowing CO_2 into and through the reaction chamber,

pressurizing the reaction chamber at a pressure less than about 2 torr, and

energizing the reaction chamber with low frequency RF power of at least about 100 watts; and

forming a dielectric layer over the SiOC layer.

55. (New) The method of claim 54, wherein the SiC layer is formed in the reaction chamber using an SiC formation process comprising:

flowing substantially pure trimetholsilane (3MS) into and through the reaction chamber; and

pressurizing the reaction chamber at a pressure less than about 2 torr.

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In the Claims:

1. (Currently Amended) A structure for providing a bond area and a probe area on a semiconductor chip, comprising:

a metal line;

an interconnect formed through a dielectric layer connecting to the metal line;

a bond pad on said semiconductor chip having a first portion disposed over the metal line and the interconnect, and a second portion disposed over the dielectric layer and offset from the metal line;

the first portion of said bond pad including a bond area for providing an attachment point for connecting a bond wire; ~~a connection; and~~

a bond wire connected to said bond area; and

the second portion including a probe area for providing contact with a probe, wherein [[the]] said bond wire connected to said bond area and said second portion coexist on said semiconductor chip.~~area is separated from the probe area.~~

2. (Previously Presented) The semiconductor chip as recited in claim 1, wherein the metal line includes copper.

3. (Previously Presented) The semiconductor chip as recited in claim 1, wherein the bond pad includes aluminum.

4. (Previously Presented) The semiconductor chip as recited in claim 1, further comprising a barrier layer disposed between the interconnect and the metal line to prevent diffusion

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therebetween.

5. (Previously Presented) The semiconductor chip as recited in claim 1, wherein the bond pad includes a thickness of less than about 2 microns.

6. (Previously Presented) The semiconductor chip as recited in claim 1, further comprising a passivation layer formed on at least a portion of the bond pad to protect the bond pad.

7. (Previously Presented) The semiconductor chip as recited in claim 6, wherein the passivation layer includes a first opening for the bond area and a second opening for the probe area.

8. (Previously Presented) The semiconductor chip as recited in claim 6, wherein the passivation layer includes an opening shared by the bond area and the probe area.

9. (Cancel)

10. (Currently Amended) A structure for providing a bond area and a probe area on a semiconductor chip, defined within a perimeter, and wherein said defined perimeter does not include separating scribe lines, comprising:

a metal layer patterned to form at least one metal line;

a dielectric layer formed on the metal layer and patterned to form a via to the at least one metal line;

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a barrier layer formed in contact with the at least one metal line through the via;

an interconnect formed in the via and connecting to the at least one metal line through the barrier layer;

a bond pad on said semiconductor chip having a first portion disposed over the at least one metal line and the interconnect, and a second portion disposed over the dielectric layer and offset from the at least one metal line said first and second portions of said bond pad located within said perimeter;

the second portion of said bond pad including said probe area, said probe area ~~on said semiconductor chip~~ for providing contact with a probe for device testing; and

the first portion of said bond pad including said bond area, said bond area ~~on said semiconductor chip~~ for providing an attachment point for a bond wire~~, wherein the bond area is separate from the probe area~~.

11. (Previously Presented) The semiconductor chip as recited in claim 10, wherein the metal layer includes copper.

12. (Previously Presented) The semiconductor chip as recited in claim 10, wherein the bond pad includes aluminum.

13. (Previously Presented) The semiconductor chip as recited in claim 10, wherein the barrier layer includes Ta or TaN.

14. (Previously Presented) The semiconductor chip as recited in claim 10, wherein the bond

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pad includes a thickness of less than about 2 microns.

15. (Previously Presented) The semiconductor chip as recited in claim 10, further comprising a passivation layer formed on the bond pad.

16. (Previously Presented) The semiconductor chip as recited in claim 15, wherein the passivation layer includes a first opening for the bond area and a second opening for the probe area.

17. (Previously Presented) The semiconductor chip as recited in claim 15, wherein the passivation layer includes an opening shared by the bond area and the probe area.

18. (Currently Amended) A structure for providing a bond area and a probe area that are still present on a semiconductor chip after separation of the chip from a wafer, comprising:

a copper layer patterned to form at least one metal line;

a dielectric layer formed on the copper layer and patterned to form a via to the at least one metal line;

a diffusion barrier layer formed in contact with the at least one metal line through the via;

an aluminum interconnect formed in the via and connecting to the at least one metal line through the diffusion barrier layer, the diffusion barrier layer for preventing atomic mixing between the at least one metal line and the aluminum interconnect;

a bond pad on said semiconductor chip integrally formed with the interconnect and having a first portion disposed over the at least one metal line and the interconnect, and a second

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portion disposed over the dielectric layer and offset from the at least one metal line;

the second portion including said probe area on said semiconductor chip for providing contact with a probe for testing the semiconductor IC chip, and wherein said probe area is still present on said semiconductor chip after separation from said wafer; and

the first portion including said bond area on said semiconductor chip for providing an attachment point for a bond wire~~, wherein the bond area is separate for the probe area~~.

19. (Previously Presented) The semiconductor chip as recited in claim 18, wherein the barrier layer includes Ta or TaN.

20. (Previously Presented) The semiconductor chip as recited in claim 18, wherein the bond pad includes a thickness of less than about 2 microns.

21. (Previously Presented) The semiconductor chip as recited in claim 18, further comprising a passivation layer formed on the bond pad.

22. (Previously Presented) The semiconductor chip as recited in claim 21, wherein the passivation layer includes a first opening for the bond area and a second opening for the probe area.

23. (Previously Presented) The semiconductor chip as recited in claim 21, wherein the passivation layer includes an opening shared by the bond area and the probe area.

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24. (New) The semiconductor chip of claim 18 further comprising a bond wire attached to said bond area.

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